What is claimed is:

1. An inverting delay component, comprising:

an inverting portion having an input terminal for receiving an input signal, a complementary input terminal for receiving a complement of the input signal, an output terminal for providing an output signal, and a complementary output terminal for providing a complement of the output signal, the inverting portion performing an inverting function such that the output signal is an inverted version of the complement of the input signal, and the complement of the output signal is an inverted version of the input signal; and

a delay control portion, comprising:

a first current source having a first impedance, the first current source coupled to the complementary output terminal and also coupled to receive a control signal;

a first resistive element coupled to the first current source, the first resistive element causing the first current source to exhibit an output impedance which is much larger than the first impedance;

a second current source having a second impedance, the second current source coupled to the output terminal and also coupled to receive the control signal; and

a second resistive element coupled to the second current source, the second resistive element causing the second current source to

exhibit an output impedance which is much larger than the second impedance.

2. The component of claim 1, wherein the first current source comprises a first transistor having a drain terminal coupled to the complementary output terminal, a gate terminal coupled to receive the control signal, and a source terminal coupled to the first resistive element.

3. The component of claim 2, wherein the second current source comprises a second transistor having a drain terminal coupled to the output terminal, a gate terminal coupled to receive the control signal, and a source terminal coupled to the second resistive element.

4. The component of claim 3, wherein the first resistive element comprises a first resistor and the second resistive element comprises a second resistor.

5. The component of claim 3, wherein the first resistive element comprises a third transistor biased to behave like a resistor, and the second resistive element comprises a forth transistor biased to behave like a resistor.

6. The component of claim 1, wherein the inverting portion comprises:

a first transistor having a gate terminal coupled to the input terminal, a drain terminal coupled to the complementary output terminal, and a source terminal coupled to a first node;

a second transistor having a gate terminal coupled to the complementary input terminal, a drain terminal coupled to the output terminal, and a source terminal coupled to the first node;

a third transistor having a gate terminal coupled to the output terminal, a drain terminal coupled to the complementary output terminal, and a source terminal coupled to the first node; and

a fourth transistor having a gate terminal coupled to the complementary output terminal, a drain terminal coupled to the output terminal, and a source terminal coupled to the first node.

7. The component of claim 6, wherein the inverting portion further comprises:

a fifth transistor having a gate terminal coupled to the complementary output terminal, a drain terminal coupled to the complementary output terminal, and a source terminal coupled to the first node; and

a sixth transistor having a gate terminal coupled to the output terminal, a drain terminal coupled to the output terminal, and a source terminal coupled to the first node.

8. The component of claim 7, wherein the first current source comprises a seventh transistor having a drain terminal coupled to the complementary output terminal,

a gate terminal coupled to receive the control signal, and a source terminal coupled to the first resistive element, and wherein the second current source comprises an eighth transistor having a drain terminal coupled to the output terminal, a gate terminal coupled to receive the control signal, and a source terminal coupled to the second resistive element.

9. The component of claim 8, wherein the first resistive element comprises a first resistor, and wherein the second resistive element comprises a second resistor.

10. The component of claim 8, wherein the first resistive element comprises a ninth transistor biased to behave like a resistor, and the second resistive element comprises a tenth transistor biased to behave like a resistor.

11. An oscillator, comprising:

an n number of inverting delay components coupled in series to form a closed loop circuit, where n is an odd integer greater than one, each inverting delay component comprising:

an inverting portion having an input terminal for receiving an input signal, a complementary input terminal for receiving a complement of the input signal, an output terminal for providing an output signal, and a complementary output terminal for providing a complement of the output signal, the inverting portion performing an inverting function such that the output signal is an inverted version of the

complement of the input signal, and the complement of the output signal is an inverted version of the input signal; and

a delay control portion, comprising:

a first current source having a first impedance, the first current source coupled to the complementary output terminal and also coupled to receive a control signal;

a first resistive element coupled to the first current source, the first resistive element causing the first current source to exhibit an output impedance which is much larger than the first impedance;

a second current source having a second impedance, the second current source coupled to the output terminal and also coupled to receive the control signal; and

a second resistive element coupled to the second current source, the second resistive element causing the second current source to exhibit an output impedance which is much larger than the second impedance;

wherein the input terminal and the complementary input terminal are coupled to a complementary output terminal and an output terminal, respectively, of a preceding inverting delay component, and

wherein the output terminal and the complementary output terminal are coupled to a complementary input terminal and an input terminal, respectively, of a succeeding inverting delay element.

12. The oscillator of claim 11, wherein the first current source comprises a first transistor having a drain terminal coupled to the complementary output terminal, a gate terminal coupled to receive the control signal, and a source terminal coupled to the first resistive element.

13. The oscillator of claim 12, wherein the second current source comprises a second transistor having a drain terminal coupled to the output terminal, a gate terminal coupled to receive the control signal, and a source terminal coupled to the second resistive element.

14. The oscillator of claim 13, wherein the first resistive element comprises a first resistor and the second resistive element comprises a second resistor.

15. The oscillator of claim 13, wherein the first resistive element comprises a third transistor biased to behave like a resistor, and the second resistive element comprises a forth transistor biased to behave like a resistor.

16. The oscillator of claim 11, wherein the inverting portion comprises:

a first transistor having a gate terminal coupled to the input terminal, a drain terminal coupled to the complementary output terminal, and a source terminal coupled to a first node;

a second transistor having a gate terminal coupled to the complementary input terminal, a drain terminal coupled to the output terminal, and a source terminal coupled to the first node;

a third transistor having a gate terminal coupled to the output terminal, a drain terminal coupled to the complementary output terminal, and a source terminal coupled to the first node; and

a fourth transistor having a gate terminal coupled to the complementary output terminal, a drain terminal coupled to the output terminal, and a source terminal coupled to the first node.

17. The oscillator of claim 16, wherein the inverting portion further comprises:

a fifth transistor having a gate terminal coupled to the complementary output terminal, a drain terminal coupled to the complementary output terminal, and a source terminal coupled to the first node; and

a sixth transistor having a gate terminal coupled to the output terminal, a drain terminal coupled to the output terminal, and a source terminal coupled to the first node.

18. The oscillator of claim 17, wherein the first current source comprises a seventh transistor having a drain terminal coupled to the complementary output terminal,

a gate terminal coupled to receive the control signal, and a source terminal coupled to the first resistive element, and wherein the second current source comprises an eighth transistor having a drain terminal coupled to the output terminal, a gate terminal coupled to receive the control signal, and a source terminal coupled to the second resistive element.

19. The oscillator of claim 18, wherein the first resistive element comprises a first resistor, and wherein the second resistive element comprises a second resistor.

20. The oscillator of claim 18, wherein the first resistive element comprises a ninth transistor biased to behave like a resistor, and the second resistive element comprises a tenth transistor biased to behave like a resistor.